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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,171	12/07/2001	Jean Louis Calvignac	RAL920010016US1	5856

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EXAMINER	
BULLOCK JR, LEWIS ALEXANDER	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/017,171	CALVIGNAC ET AL.	
	Examin r	Art Unit	
	Lewis A. Bullock, Jr.	2195	

-- The MAILING DATE of this communicati n appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,10-14,17 and 18* is/are rejected.

7)☒ Claim(s) *6-9,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 10, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by AMBROSIUS (U.S. Patent 4,527,233).

As to claim 10, AMBROSIUS teaches a communication parallel processing method including the acts of: providing at least one process engine (controller / host CPU being able to perform various computing functions) (col. 2, lines 4-6; col. 2, lines 14-19) that provides a predetermined task; providing at least one buffer operatively coupled to the process engine and to an input bus (via the buffer RAM being connected to the data base to the CPU and to the controller) (col. 2, lines 25-29); putting the at least one buffer in a fast write mode wherein data is received and written into the buffer at a first speed (via using the host write enable signal to transfer data to and from the CPU) (col. 2, lines 34-45; col. 2, lines 53-55); putting the buffer in a slow read mode wherein data is read from the buffer into the at least one process engine at a second speed (via using the controller read enable signal to transfer data between the disk drive and the buffer RAM) (col. 2, lines 46-55); activating the at least one process engine to process data read out of the buffer (via receiving or sending the data); putting the at least one buffer in slow write mode wherein processed data is written into the

buffer from the at least one process engine at a third speed (via using the controller write enable signal to transfer data) (col. 2, lines 46-55); and putting the at least one buffer in a fast read mode wherein processed data is read out of the buffer at the same speed and sequence as the speed and sequence at which the data was received from the input bus (via using the host read enable signal to transfer/read data in a sequence) (col. 2, lines 34-45; col. 2, lines 53-55; col. 3, lines 15-32; col. 4, lines 32-67).

As to claim 12, AMBROSIUS teaches a communication system (data processing system) comprising: at least one buffer (buffer system / RAM) having a first connection that ports to a network (bus), a second connection that ports to a network (bus), a third connection that ports to a process (controller) and a fourth connection that ports to the processor (CPU) (see the figure); and a control circuit including a time division multiplexor that generates a Fast Write Phase in which data is received at the first connection at a first speed (via using the host write enable signal to transfer data to and from the CPU) (col. 2, lines 34-45; col. 2, lines 53-55), a Slow Read Phase at which data is transferred from the buffer through the third connection at a second speed (via using the controller read enable signal to transfer data between the disk drive and the buffer RAM) (col. 2, lines 46-55), a Slow Write Phase in which data is written form the fourth connection into the buffer a the second speed (via using the controller write enable signal to transfer data) (col. 2, lines 46-55) and a Fast Read Phase in which data is transferred from the buffer to the second connection at the first speed in the same order that the data was received (via using the host read enable signal to transfer/read

data in a sequence) (col. 2, lines 34-45; col. 2, lines 53-55; col. 3, lines 15-32; col. 4, lines 32-67).

As to claim 13, AMBROSIUS teaches a process engine operatively coupled to the third connection and the fourth connection (via the CPU and controller both control the transfer of data to he disk drive and thereby performing a processing function) (see figure).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over AMBROSIUS (U.S. Patent 4,527,233).

As to claim 11, AMBROSIUS substantially discloses the invention above. However, AMBROSIUS does not teach that the function is cryptographic. Official Notice is taken in that it is well known in the art that data transferring for storage would involve encrypting the data when it is transferred over a network and therefore it would be obvious to one of ordinary skill in the art that the data is encrypted / decrypted when transferred to / from a data storage device. For instance see U.S. Patent 4,809,171 DOZIER wherein data transferred from a processing unit from one bus is sent to

another operation circuit that performs processing of the data, i.e. shifts, logical ANDS, data modification functions, etc. to a memory device.

As to claim 14, AMBROSIUS substantially discloses the invention above. However, AMBROSIUS does not teach that the function is cryptographic. Official Notice is taken in that it is well known in the art that data transferring for storage would involve encrypting the data when it is transferred over a network and therefore it would be obvious to one of ordinary skill in the art that the data is encrypted / decrypted when transferred to / from a data storage device. For instance see U.S. Patent 4,809,171 DOZIER wherein data transferred from a processing unit from one bus is sent to another operation circuit that performs processing of the data, i.e. shifts, logical ANDS, data modification functions, etc. to a memory device.

5. Claims 1-3, 5, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over DOZIER (U.S. Patent 4,809,171) in view of AMBROSIUS, III (U.S. Patent 4,527,233).

As to claim 1, DOZIER teaches a communication parallel processing system comprising: an input bus (input bus) (see figure 1); N task oriented processing devices (operation circuits) (see figure 1), wherein N is greater than 1 and each of the task-oriented devices providing a particular function (see figure 1; col. 2, lines 52-65) such that the processing devices output the results to an output bus in the order that inputs

were outputted on the input bus (col. 2, lines 52-65). However, DOZIER does not teach the buffers connected to the input bus.

AMBROSIUS teaches a controller performing a function on data sent on input bus and sending data to be stored or retrieved to/from a disk drive which connected to the controller over another communication wherein the buffers connected to the input bus, M greater than 1, each one adaptable to operate in a plurality of different phases operatively coupled to the task oriented processing device; and Time Division Multiplex Control mechanisms operatively connected to the M buffers and imposing respective ones of the different phases on the M buffers to deliver outputs from the buffers to an output bus (connection of the disk drive) in the order that inputs were outputted on the input bus (via using the host read enable signal / host write enable signal / controller write enable signal / controller read enable signal to transfer / read data in a sequence) (col. 2, lines 34-55; col. 3, lines 15-32; col. 4, lines 32-67). It would be obvious that each operation circuit in DOZIER would constitute a controller of AMBROSIUS since both the operating circuit and the controller enhance processing speed and generate results that are sent to memory. Therefore, it would be obvious to combine the teachings of DOZIER with the teachings of AMBROSIUS in order to facilitate control over the rate data is transferred (col. 1, lines 26-36; col. 1, lines 39-56).

As to claim 2, It would be obvious that since there are no limits to the maximum amount of processing devices and buffers, that it would be obvious to one of ordinary skill in the art that both are equal.

As to claims 3, 17 and 18, DOZIER wherein data transferred from a processing unit from one bus is sent to another operation circuit that performs processing of the data, i.e. shifts, logical ANDS, data modification functions, etc. wherein the data is sent to a memory device. Official Notice is taken in that data modification is a form of encrypting data and therefore the function would constitute cryptography.

As to claim 5, AMBROSIUS teaches the plurality of different phases include a Fast Write Phase (via using the host write enable signal to transfer data to and from the CPU) (col. 2, lines 34-45; col. 2, lines 53-55), a Slow Read Phase (via using the controller read enable signal to transfer data between the disk drive and the buffer RAM) (col. 2, lines 46-55), a Slow Write Phase (via using the controller write enable signal to transfer data) (col. 2, lines 46-55) and a Fast Read Phase (via using the host read enable signal to transfer/read data in a sequence) (col. 2, lines 34-45; col. 2, lines 53-55; col. 3, lines 15-32; col. 4, lines 32-67).

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention. The last putting limitation details "putting the at least one buffer in a fast **write** mode wherein processed data is read out of the buffer at the same speed...". The bold language should be "read" not "write". Otherwise Applicant provides to different functionalities that occur based on the buffer being in a fast write mode operating a different speeds that would be impossible.

Allowable Subject Matter

8. Claims 6-9, 15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

May 30, 2006

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER